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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,105	11/14/2003	Anthony Correale JR.	RPS920030130US1	1935
25299	7590	07/20/2007		
IBM CORPORATION PO BOX 12195 DEPT YXSA, BLDG 002 RESEARCH TRIANGLE PARK, NC 27709			EXAMINER PATEL, KAUSHIKKUMAR M	
			ART UNIT 2188	PAPER NUMBER
			MAIL DATE 07/20/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/714,105	Applicant(s) CORREALE ET AL.	
	Examiner Kaushikkumar Patel	Art Unit 2188	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 12 July 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ They raise the issue of new matter (see NOTE below);
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).


4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: _____.
Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See continuation sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____.
13. ☐ Other: _____.


HYUNG SOUH
SUPERVISORY PATENT EXAMINER
7/19/07

Applicant argues that Aoki, Shirotori and Santhanam (or Huang) does not teach applying/supplying clock pulses/signals to one or both ways in response to an access mode signal, a HIT A signal and a HIT B signal (remarks, pages 8, 10 and 12). Below is a comparison between embodiments of applicant's invention with Shirotori. (left side, applicant's fig. 1 and right side, Shirotori, fig.3).



As can be seen from above comparison, that applicant's HIT A and HIT B signals are equivalent to signal output by Hit Controller (Shirotori, item 4). Applicant's HIT A and HIT B signals are supplied to multiplexer 25 to select data from way 0 or way 1, similarly Shirotori's Hit Controller supplies signals to way selector to select data from data

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memories (i.e. ways). Applicant's hit signals also applied to clock supply circuit (item, 20) which enables either way 0 or way 1, similarly Shirotori's hit signals are applied to access controller (item 8), which enables either 0th way or (n-1)th way. Applicant's clock circuit receives access mode signal similar to Shirotori's start signal. Thus, from above side-by-side comparison of applicant's embodiment with Shirotori reveals that the access controller (item 8) performs similar function as of applicant's clock supply circuit (i.e. enables either way 0 or way 1). Applicant argues that Shirotori initially supplies enable signal to both ways and then stops supplying enable signal (remarks, page 9). Examiner respectfully disagrees with that and presents following comparison between applicant's disclosure to Shirotori's disclosure:

Applicant discloses: "When the access cycle is slow enough to permit a single way to be clocked, and data is produced prior to the end of the access cycle (i.e. hit is generated early), only one of the ways (shown as way 0 in FIG. 2) is clocked if a hit is determined" (page 7, par. 21) and "When the microcomputing system is running an application which permits the power efficiency mode to operate, based on an assessment that sufficient cycle time is available to permit identification of the way containing the data defined by the line index of the effective address 19, only one of the ways 21 is clocked if a hit is determined" (page 8, par. 23). **Shirotori discloses:** "According to the start signal from the start signal generator 7 and the hit information from the hit controller 4, the access controller 8 supplies an enable signal for allowing the reading of data out of one of the data memories 2 that is associated with the hit tag memory 1. If the access controller 8 receives the hit information before the start

signal, it supplies the enable signal **only to the data memory 2** associated with the hit tag memory 1." (Shirotori, col. 4, line 64 – col. 5, line 1). What applicant pointed out on page 9 of remarks page is "if hit information is not received early" condition, which is absent in applicant's disclosure. As explained above, Shirotori teaches enabling one of the cache ways to be selected but fails to teach enabling cache way with clock supply circuit and to supplement that limitation Santhanam was introduced. Santhanam teaches enabling/disabling a cache way by providing or not providing clock signal (Santhanam, par. [0057], [0058]). Applicant further argues that Santhanam teaches conditionally clocking bank (or way) of cache based on load/store instruction, but it is apparently true because data is always accessed based on load/store instruction. Huang also teaches gated clock circuit to enable/disable one of the cache ways to reduce power consumption (Huang, page 13, left col.).

Thus, from above explanation it is apparently clear that applicant's arguments are non-persuasive.